IN THE CLAIMS

1. (currently amended) A process for fabricating an electronic device, the process comprising:

(a.) forming a first dopant blocking layer at a first temperature; and

(b.) forming a second dopant blocking layer at a second temperature over said first dopant blocking layer,

said first and second dopant blocking layers being disposed between a semi-insulating layer and a p-type layer.

2. (original) A process as recited in claim 1, wherein said first temperature is lower than said second temperature.

3. (original) A process as recited in claim 1, wherein the process further comprises:

forming a third dopant blocking layer between said first and said second dopant blocking layers.

4. (original) A process as recited in claim 1, wherein said first dopant blocking layer is formed over a vertical sidewall of a mesa and over a horizontal surface of a substrate; and

said first dopant blocking layer has a substantially uniform thickness.

5. (original) A process as recited in claim 1, wherein said first and said second blocking layers are InAlAs.

6. (original) A process as recited in claim 3, wherein said third dopant blocking layer is chosen from the group consisting essentially of InP, InGaP, InGaAs, or InGaAsP .

7. (original) A process as recited in claim 1, wherein said first temperature lies in the range of approximately 500°C to approximately 570°C.

8. (original) A process as recited in claim 4, wherein said thickness is in the range of approximately 50 nm to approximately 100 nm.

9. (original) A process as recited in claim 1, wherein said second dopant blocking layer has a vertical portion and said vertical portion has a thickness in the range of approximately 30 nm to approximately 100 nm.

10. (original) A process as recited in claim 1, wherein said first and second dopant blocking layers are InGaAlAs.

11. (original) A process as recited in claim 1, wherein said first dopant blocking layer is disposed above a p-type layer and said second dopant blocking layer is disposed below a semi-insulating layer.

12. (original) A process a recited in claim 1, wherein said first dopant blocking layer is disposed below a p-type layer and said second dopant blocking layer is disposed above a semi-insulating layer.

13. (original) A process for fabricating an optoelectronic device as recited in claim 1, wherein said second temperature lies in the range of approximately 600° C to approximately 650° C.

14. (previously amended) A process as recited in claim 1, wherein said first and said second dopant blocking layers are formed by MOVPE.

15. (previously amended) A process as recited in claim 1, wherein said first and said second dopant blocking layers are formed by MBE.

16. (original) A process as recited in claim 15, wherein said first temperature lies in the range of approximately 400° C to approximately 470° C.

17. (original) A process as recited in claim 15, wherein said second temperature lies in the range of approximately 500° C to approximately 550° C.

18. (original) A process as recited in claim 14, wherein said first temperature is in the range of approximately 500° C to approximately 570° C.

19. (original) A process as recited in claim 14, wherein said second temperature lies in the range of approximately 600 ° C to approximately 650 ° C.

20. (currently amended) A process for fabricating an electronic device, the process comprising:

(a.) forming a first InAlAs layer at a first temperature; and

(b.) forming a second InAlAs layer at a second temperature over said first InAlAs layer,

said first and second InAlAs layers being disposed between a semi-insulating layer and a p-type layer .

21. (original) A process as recited in claim 20, wherein said first temperature is lower than said second temperature.

22. (original) A process as recited in claim 20, wherein the process further 2 comprises:
forming a layer of undoped InP between said first and said second InAlAs layers.

23. (original) A process as recited in claim 20, wherein said first InAlAs layer is formed over a vertical sidewall of a mesa and over a horizontal surface of a substrate; and wherein said first InAlAs layer has a substantially uniform thickness.

24. (original) A process as recited in claim 20, wherein said first InAlAs layer is disposed above a p-type layer and said second InAlAs layer is disposed below a semi-insulating layer.

25. (original) A process a recited in claim 20, wherein said first InAlAs layer is disposed below a p-type layer and said second InAlAs layer is disposed above a semi-insulating layer.

26. (original) A process for fabricating an electronic device as recited in claim 20, wherein said second temperature lies in the range of approximately 600°C to approximately 650 °C.

27. (original) A process as recited in claim 20, wherein said first temperature lies in the range of approximately 500 °C to approximately 570 °C.

28. (original) A process as recited in claim 20, wherein said first and said second dopant blocking layers are formed by MOVPE.

29. (original) A process as recited in claim 20, wherein said first temperature lies in the range of approximately 400 °C to approximately 470 °C.

30. (original) A process as recited in claim 20, wherein said second temperature lies in the range of approximately 500° C to approximately 550° C.

31. (original) A process as recited in claim 20 wherein said first and said second dopant blocking layers are formed by MBE.

Claims 32-58 (CANCELLED)

59 (cancelled)

60. (currently amended) A process as recited in claim ~~59~~ 1 wherein the p-type layer includes a Zn dopant, and the semi-insulating layer includes an Fe dopant.

61 (cancelled)

62. (currently amended) A process as recited in claim ~~61~~ 20 wherein the p-type layer includes a Zn dopant, and the semi-insulating layer includes an Fe dopant.